ABSTRACT

The present invention provides a semiconductor integrated circuit capable of testing a high-speed memory at the actual operation speed of the memory even when the operation speed of the BIST circuit of the integrated circuit is restricted.

In order to test a memory operating on a first clock, the integrated circuit is provided with a first test pattern generation section, operating on a second clock, for generating test data, and a second test pattern generation section, operating on a third clock, the inverted clock of the second clock, for generating test data. Furthermore, the integrated circuit is provided with a test data selection section for selectively outputting either the test data output from the first test pattern generation section or the test data output from the second test pattern generation section depending on the signal value of the second clock, thereby inputting the test data to the memory as test data. The frequency of the second clock is half the frequency of the first clock.